27.2 1/2-inch 7.2MPixel CMOS Image Sensor with 2.25μm Pixels Using 4-Shared Pixel Structure for Pixel-Level Summation

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In recent years, the market for CMOS image sensors (CIS) have been rapidly growing in several high-volume applications, such as mobile phones, digital still cameras (DSC), and camcorders. This growth in not only due to the ability to integrate sensing array with analog- and digital-processing circuits in CMOS, but also the persistently improving image quality of CIS that is comparable to that of CCD [1]. In addition, the pixel size of CIS has been reduced and become comparable to CCD with the help of pixel-sharing architecture that results in the high capacity of photodiode and thus, the high SNR even with the small-size pixel. Although the image quality and the pixel size of CIS are comparable to CCD, the SNR of CIS under the preview and sub-sampling operation for recording a moving object is not as good as that of CCD. This is because the signal charge of CCD under sub-sampling mode can be added up at the vertical-CCD stage and thus, the SNR increases compared with full-resolution mode whereas that is not the case for previously reported CIS. In this paper, a $^1/_2$-inch 7.2MPixel CIS with 2.25μm pixel is described using 4-shared pixel structure realizing pixel-level charge summation function, similar to CCD. This resulting pixel having 57% fill factor shows full well capacity of 14,000e$^-$ with SNR_{max} of 41dB under the full-resolution operation, and an additional 6dB increment of SNR by the pixel-level charge summation under sub-sampling operation. A Cu process with 0.13μm design rule and a low-noise process technology are employed for high sensitivity of 15,000e$^-$/lux.s and low noise of 8e$^-$, respectively.

Figure 27.2.1 depicts the schematic diagram and basic timing of a 4-shared pixel architecture. Four photodiodes are sharing a source follower (SF), a reset-gate (RG) transistor, and a selection (SEL) transistor over 4 pixels grouped in the vertical direction, resulting in 1.75 transistors per a pixel. This 4-shared 2.25μm pixel, combined with an advanced 0.13μm Cu process achieves a conversion gain of 40μV/e, a fill factor of 57%, and a full-well capacity of 14,000e$^-$. This way of sharing 4 pixels in the vertical direction has two strong advantages compared to the previous shared architecture [2]. First, it can be read out one row at a time, like the case of non-shared structure that can reduce FPN between even and odd columns arising from the readout timing asymmetry in the 4-shared structure using 2 columns for sharing. Second, when the whole pixel image array is sub-sampled by 4 times, like preview or sub-sizing, some pixels are conventionally skipped during readout (Fig. 27.2.2), thus, losing surrounding 75% image information. However, the structure in Fig. 27.2.1 makes it possible to sum up the charges in 2 same-colored photodiodes into its corresponding shared floating diffusion (FD) node, simply by turning on 2 TGs simultaneously, at the pixel level, similar to CCD. These vertically summed charge data of one row are moved to correlated-double sampling (CDS) domain, where the averaging of the adjacent 2 columns is conducted horizontally. Consequently, 6dB improvement of SNR can be achieved by 4-times increment of signal charges. Figure 27.2.3 shows that the SNR improvement achieved by the pixel-level charge summation is more than 5.3dB compared to conventional sub-sampling. This function can offer improved image quality at sub-sampling operation such as motion recording, without any additional memory as well as the loss of read-out and image processing time.

Although the FPN of CIS is reduced to an acceptable level through the help of the CDS technology, however, its random noise has still deteriorated the image quality compared to CCDs which sets limit on SNR in low illumination and dynamic range. Major source of dark random noise has been previously proven to be flicker noise in SF due to the interface trap between gate oxide and silicon channel [3]. The gate oxide fabrication process is changed to reduce the interface trap density of SF transistor. In conventional GNOX process (Fig. 27.2.4), to prevent boron segregation from silicon to gate poly, gate oxidation is formed at high temperature in nitrogen atmosphere. In this case, nitrogen ions spread out from gate oxide to silicon surface due to its diffusion, so that trapping probability of signal electrons in the channel increases, causing flicker noise. To reduce the trapping effect of nitrogen ion, a nitrogen film has been formed under low temperature condition so that the nitrogen ion can be localized far from the oxide-silicon interface. As shown in Fig. 27.2.4, compared with GNOX method, dark random noise can be decreased by 40% through this process, with the result that the asymmetric behavior due to the high 1/f noise has been reduced in dark state histogram.

As the pixel size shrinks and the pixel array becomes larger, the distance between micro-lens and photodiode becomes increasingly important in the viewpoints of light-gathering efficiency and crosstalk. A Cu process with 0.13μm design rule technology is used to reduce the pixel height by 20%, through the smaller thickness of metal and inter-layer materials compared with that of Al, as shown in Fig. 27.2.6. The multiple interfaces of inter-layer materials resulting from Cu damascene process, which degrade the sensitivity performance due to the optical reflection phenomena at each interface, have been removed out by the additional cavity process, resulting in increased optical sensitivity up to 15,000e$^-$/lux.s.

Figures 27.2.6, and 27.2.7 show the captured image of full resolution of 7.2MPixel array, together with optical and electrical characteristics of the 2.25μm pixel.

References:

[1] A. El Gamal and H. Eltoukhy, "CMOS Image Sensor," *IEEE Circuit and Devices Magazine*, vol. 21, no. 3, pp. 6-20, May-June, 2005.

[2] M. Mori, et al., "A 1/4 inch 2M Pixel CMOS Image Sensor with 1.75 Transistor/Pixel," *ISSCC Dig. Tech. Papers*, pp. 110-111, Feb., 2004.

[3] J.Y. Kim, et al., "Characterization and Improvement of Random Noise in 1/3.2" UXGA CMOS Image Sensor with 2.8μm Pixel using 0.13μm Technology," *IEEE Charge-Coupled Devices and Advanced Image Sensors*, pp. 149-152, 2005.

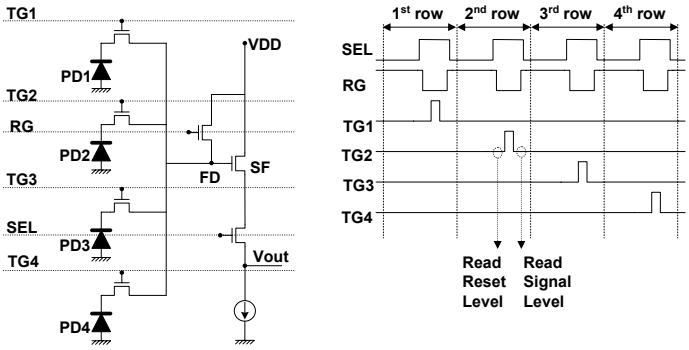


Figure 27.2.1: Schematic of 4-shared APS and its basic timing than can realize the pixel-level sub-sampling.

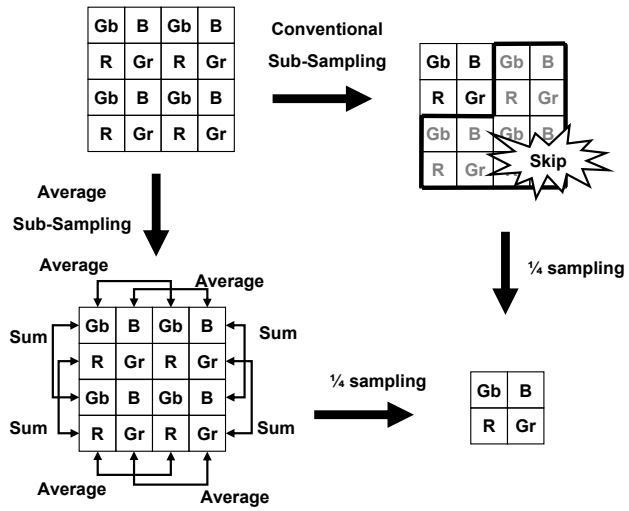
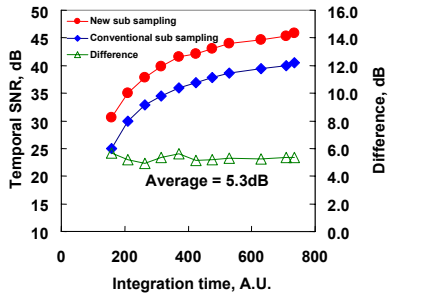


Figure 27.2.2: Pixel-level charge summation for sub-sampling.



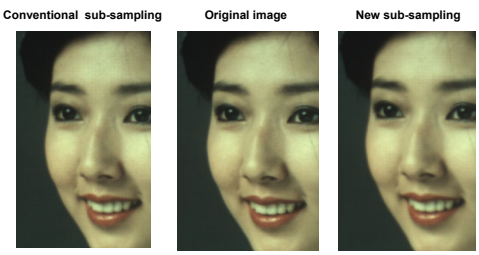


Figure 27.2.3: SNR Increase with new sub-sampling.

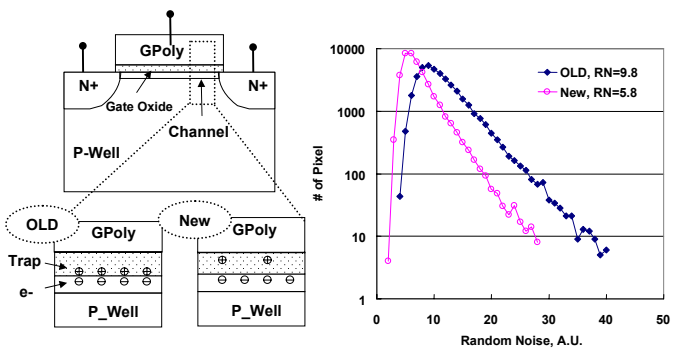


Figure 27.2.4: Old and new GNOX process; improvement of random noise by reducing the trap effect on SF transistor.

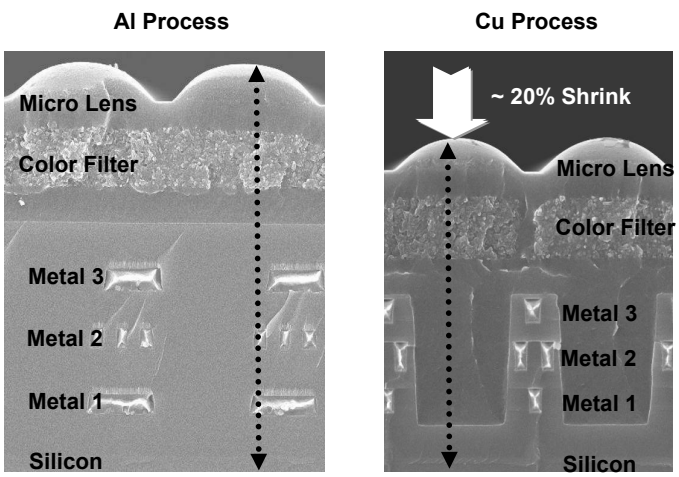


Figure 27.2.5: Vertical structure of Cu process.

	characteristics
Pixel Resolution	7.2M
Pixel Size	2.25μm
SNRmax	41.4 dB @ full resolution 46.7 dB @ sub sampling
Full Well Capacity	14,000 e⁻ @ full resolution 28,000 e⁻ @ sub sampling
Sensitivity @ G channel	15000 e⁻ /lux.sec @ full resolution 30000 e⁻ /lux.sec @ sub sampling
Random noise	8 e-
ADC Resolution	13b
Frame Rate	7.7frames/s
Conversion Gain (FD)	40μV/e
Dark current (@ 40 degree)	15e/s

Figure 27.2.6: Measured pixel characteristics.

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Figure 27.2.7: Captured 7.2M full image.

